Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate ~~having an integrated circuit thereon~~ and including a lower electrode, a dielectric [[film]] layer, and an upper electrode, said dielectric [[film]] layer being formed from ~~either a dielectric material having a high dielectric constant or~~ a ferroelectric material;

a first interlayer insulating [[film]] layer provided so as to ~~directly~~ cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating [[film]] layer and electrically connected to ~~the integrated circuit and~~ the capacitor through a first contact hole formed in the first interlayer insulating [[film]] layer;

a second interlayer insulating [[film]] layer consisting of an interlayer insulating film having a tensile stress provided on ~~so as to directly cover~~ the first interconnect ~~and the first interlayer insulating film~~; and

a second interconnect selectively provided on the second interlayer insulating [[film]] layer and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating [[film]] layer~~; and~~

~~a passivation layer provided so as to cover the second interconnect, wherein the second interconnect is provided on the second interlayer insulating film so as to cover at least a part of the capacitor~~.

2.-3. (Cancelled).

4. (Currently Amended) A semiconductor device according to claim 1, ~~wherein~~ further comprising,

a passivation layer provided so as to cover the second interconnect, wherein the second interconnect is provided on the second interlayer insulating film so as to cover at least a part of the capacitor,

the passivation layer is formed from a laminate including a silicon oxide film and a silicon nitride film.

5. (Cancelled).

6. (Original) A semiconductor device according to claim 1, wherein the first interconnect is formed from a laminate including titanium, titanium nitride, aluminum and titanium nitride; a laminate including titanium, titanium nitride and aluminum; a laminate including titanium, titanium tungsten, aluminum and titanium tungsten; or a laminate including titanium, titanium tungsten and aluminum.

7. (Currently Amended) A semiconductor device according to claim 1, wherein a Si-OH bond absorption coefficient of the second interlayer insulating [[film]] layer at a wavelength corresponding to 3450 cm^{-1} is 800 cm^{-1} or less.

8. (Currently Amended) A semiconductor device according to claim 1, wherein the second interlayer insulating [[film]] layer has a tensile stress of 1×10^7 dyn/cm^2 to 3×10^9 dyn/cm^2 inclusive.

9. (Currently Amended) A semiconductor device according to claim 1, wherein the second interlayer insulating [[film]] layer has a thickness of 0.3 μm to 1 μm inclusive.

10. (Original) A semiconductor device according to claim 1, wherein the second interconnect is formed from a laminate including titanium, aluminum and titanium nitride; a laminate including titanium and aluminum; or a laminate including titanium, aluminum and titanium tungsten.

11. (Withdrawn) A method for fabricating a semiconductor device, comprising the steps of:

sequentially forming a lower electrode, a dielectric film, and an upper electrode on a supporting substrate having an integrated circuit, thereby forming a capacitor;

forming a first interlayer insulating film so as to cover the capacitor;

forming a first contact hole in the first interlayer insulating film;

selectively forming a first interconnect in the first contact hole and on a prescribed area of the first interlayer insulating form so as to be electrically connected to the integrated circuit and the capacitor;

forming a second interlayer insulating film of ozone TEOS so as to cover the first interconnect;

subjecting the second interconnect to a first thermal treatment;

forming a second contact hole in the second interlayer insulating film;

selectively forming a second interconnect in the second contact hole and on a prescribed area of the second interlayer insulating film so as to be electrically connected to the first interconnect;

subjecting the second interconnect to a second thermal treatment; and

forming a passivation layer so as to cover the second interconnect.

12. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein the dielectric film is formed from either a dielectric material having a high dielectric constant or a ferroelectric material.

13. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, further comprising the step of etching back the second interlayer insulating film using the second interconnect as a mask to such an extent as to almost expose the first interconnect.

14. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein the step of forming the second interconnect includes the step of forming the second interconnect so as to cover at least a part of the capacitor.

15. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein:

the passivation layer is formed of a laminate including a silicon oxide film and a silicon nitride film, and

the silicon oxide film is formed by normal-pressure CVD, low-pressure CVD or plasma CVD, with using silane, disilane or ozone TEOS, so as to have a tensile stress.

16. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, further comprising the steps of:

after the first interconnect is formed, forming a hydrogen supplying layer on the first interconnect excluding an area where the capacitor is provided; and

performing a third thermal treatment.

17. (Withdrawn) A method for fabricating a semiconductor device according to claim 16, wherein the hydrogen supplying layer is formed from either silicon nitride or silicon nitride oxide by plasma CVD.

18. (Withdrawn) A method for fabricating a semiconductor device according to claim 16, wherein the third treatment performed after the formation of hydrogen supplying layer is performed at a temperature in the range of 300°C to 450°C inclusive.

19. (Withdrawn) A method for fabricating a semiconductor device according to claim 16, wherein the third treatment performed after the formation of the hydrogen supplying layer is performed in an oxygen atmosphere, a nitrogen atmosphere, an argon atmosphere or an atmosphere of a mixed gas thereof.

20. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein the first interlayer insulating film is formed of silicon oxide by normal-pressure CVD or low-pressure CVD, with using silane, disilane or ozone TEOS.

21. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein the first interlayer insulating film is formed of phosphorus-doped silicon oxide by normal-pressure DVD or low-pressure CVD.

22. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein an ozone concentration upon forming the second interlayer insulating film using ozone TEOS is set to be at 5.5% or more.

23. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein the second interlayer insulating film after being subjected with the first thermal treatment has a tensile stress of 1×10^7 dyn/cm^2 to 2×10^9 dyn/cm^2 inclusive.

24. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein the first thermal treatment is performed at a temperature in the range of 300°C to 450°C inclusive.

25. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein the first thermal treatment is performed in an atmosphere containing at least oxygen.

26. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein the second thermal treatment is performed at a temperature in the range of 300°C to 450°C inclusive.

27. (Withdrawn) A method for fabricating a semiconductor device according to claim 11, wherein the second thermal treatment is performed in an atmosphere containing at least one of nitrogen, argon and helium.

28. (Cancelled)

29. (Currently Amended) The semiconductor device of claim 1 wherein the second interlayer insulating [[film]] layer provides substantially flat step coverage of the first interconnect and the first interlayer insulating [[film]] layer.

30. (Currently Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate ~~having an integrated circuit thereon~~ and including a lower electrode, a dielectric [[film]] layer, and an upper electrode, said dielectric [[film]] layer including a remnant polarization of approximately 10 $\mu C/cm^2$;

a first interlayer insulating [[film]] layer provided so as to ~~directly~~ cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating [[film]] layer and electrically connected to ~~the integrated circuit and~~ the capacitor through a first contact hole formed in the first interlayer insulating [[film]] layer;

a second interlayer insulating [[film]] layer consisting of an interlayer insulating film having a tensile stress provided on ~~so as to directly cover~~ the first interconnect ~~and the first interlayer insulating film~~; and

a second interconnect selectively provided on the second interlayer insulating [[film]] layer and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating [[film]] layer; ~~and~~

~~a passivation layer provided so as to cover the second interconnect~~.

31. (Currently Amended) A semiconductor device, comprising:

a capacitor provided on a supporting substrate ~~having an integrated circuit thereon~~ and including a lower electrode, a dielectric [[film]] layer, and an upper electrode, said dielectric [[film]] layer including a remnant polarization of at least 10 $\mu C/cm^2$;

a first interlayer insulating [[film]] layer provided so as to ~~directly~~ cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating [[film]] layer and electrically connected to ~~the integrated circuit and~~ the capacitor through a first contact hole formed in the first interlayer insulating [[film]] layer;

a second interlayer insulating [[film]] layer consisting of an interlayer insulating film having a tensile stress provided ~~so as to directly cover~~ on the first interconnect ~~and the first interlayer insulating film~~; and

a second interconnect selectively provided on the second interlayer insulating [[film]] layer and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating layer ~~film; and~~

~~a passivation layer provided so as to cover the second interconnect~~.

32. (Cancelled).

33. (Previously Presented) A semiconductor device, comprising:

a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode, said dielectric film being formed from either a dielectric material having a high dielectric constant or a ferroelectric material;

a first interlayer insulating film provided so as to directly cover the capacitor;

a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a first contact hole formed in the first interlayer insulating film;

a second interlayer insulating film having a tensile stress provided so as to directly cover the first interconnect and the first interlayer insulating film;

a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film; and

a passivation layer provided so as to cover the second interconnect; and

a hydrogen supplying layer provided between the first interconnect and the second interlayer insulating film excluding an area in which the capacitor is provided.

34. (Previously Presented) A semiconductor device, comprising:

a capacitor provided on a supporting substrate having an integrated circuit thereon and including a lower electrode, a dielectric film, and an upper electrode;

a first interlayer insulating film provided so as to directly cover the capacitor, the first interlayer insulating film having a tensile stress;

a first interconnect selectively provided on the first interlayer insulating film and electrically connected to the integrated circuit and the capacitor through a contact hole formed in the first interlayer insulating film;

a second interlayer insulating film having a tensile stress provided so as to directly cover the first interconnect and the first interlayer insulating film;

a second interconnect selectively provided on the second interlayer insulating film and electrically connected to the first interconnect through a second contact hole formed in the second interlayer insulating film;

a passivation layer provided so as to cover the second interconnect; and

a hydrogen supplying layer provided between the first interconnect and the second interlayer insulating film excluding an area in which the capacitor is provided.

35. (New) The semiconductor device of claim 1, further comprising a passivation layer provided so as to cover the second interconnect.

36. (New) The semiconductor device of claim 1, wherein the second interlayer insulating layer being a singular layer.

37. (New) The semiconductor device of claim 1, wherein the second interlayer insulating layer forming of thermal ozone TEOS.

38. (New) The semiconductor device of claim 1, further comprising the supporting substrate having an integrated circuit thereon.